## Q.P. Code :10650

**[Time: 3 Hours]** **[Marks:80]**

Please check whether you have got the right question paper.

**N.B:**
1. Question No. 1 is **compulsory.**
2. **Attempt any three questions from remaining five questions.**
3. **Assume suitable data where required.**
4. **Figures** to the **right** indicate **full marks**.

**Q.1** **(solve Any 4)**

a] Compare NMOS & CMOS technology in VLSI design. **05**

b] Implement the following function using Dynamic CMOS logic. **05**

$$Y = \overline{A(B + C)}$$

c] Compare Ripple carry adder with CLA. **05**

d] Explain working Principle of flash memory. **05**

e] Explain importance of low power design. **05**

**Q.2** a] Compare the full scaling & constant voltage scaling models of MOSFETS. Demonstrate the effects of scaling on the area, delay, power consumption and current density of the device **10**

b] Explain transfer characteristics for NMOS. Inverter showing different regions. What is the effect of variation in W/L ratio? **10**

**Q.3** a] Draw 1T DRAM cell and explain it's write, read, hold & refresh operation. **10**

b] Explain scheme for multiplication of 101*010. **10**

**Q.4** a] Explain various techniques of clock generation & clock distribution. **10**

b] Consider a CMOS Inverter circuit with following parameters. **10**

$V_{DD}$ = 3.3v.

$V_{To,n}$ = 0.6v.

$V_{To,p}$ = -0.7v.

$K_n$ = 200 $\mu$ A|V²

$K_p$ = 80 $\mu$ A|V²

Calculate noise Margins of the circuit Consider $K_R$ = 2.5 & $V_{To,n} \neq V_{To,p}$.

**Q.5** a] Draw JK Flip Flop using. CMOS and explain the working. **10**

b] Draw CLA (carry lookahead adder) carry chain using dynamic CMOS logic. **10**

**Q.6** Write Short notes on **(any three)** **20**

a] Latch up in CMOS

b] Sense Amplifier.

c] Interconnect scaling.

d] 4*4 Barrel Shifter.

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